IN THE CLAIMS:

1. (CURRENTLY AMENDED) Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:

a plurality of processors arranged so that data advances from processor to processor during normal operation, each processor being a part of a processor complex that includes a first context memory for data to be processed, and a second context memory for data that has been processed;

an advancement circuit, the advancement circuit configured to advance ~~enabling advancement of~~ data among the processors in the event of failure of a processor; and

a data bypass circuit configured to pass the data through the processor complex with ~~past a~~ the failed one of the processors, by moving the data from the first context memory to the second context memory of that processor complex absent processing.

2. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, wherein said data bypass circuit further comprises:

a bypass register.

3. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, further comprising:

said plurality of processors arranged to process data as a pipeline.

4. (PREVIOUSLY PRESENTED) The apparatus as in claim 1, further comprising:

said plurality of processors arranged to process data as a pipeline; and

a bypass register, said bypass register having a bit location for each processor of the pipeline, each bit location capable of storing an override signal.

5. (CURRENTLY AMENDED) The apparatus as in claim 1, further comprising:

a memory, said memory storing computer code, said computer code having a code entry point selected by said data bypass circuit to enable a downstream processor to do the work of ~~a~~ the failed processor.

6. (CURRENTLY AMENDED) A method for enhancing debug capability in a multiprocessor circuit, comprising:

advancing data among a plurality of processors~~, the plurality of processors arranged so that data advances from processor to processor~~ during normal operation in response to completion signals from each of the processors;

advancing data among the processors ~~by an advancement circuit,~~ in the event of failure of a processor in response to an override signal; and

passing the data through a processor complex including the ~~past a~~ failed one of the processors by ~~a data bypass circuit~~ moving data from a first context memory to a second context memory of the processor complex absent processing.

7. (PREVIOUSLY PRESENTED) The method apparatus as in claim 6, further comprising:

indicating that a processor is to be bypassed by a bypass register.

8. (PREVIOUSLY PRESENTED) The method as in claim 6, further comprising:

arranging said plurality of processors to process data as a pipeline.

9. (CURRENTLY AMENDED) The method as in claim 6, further comprising:

arranging said plurality of processors to process data as a pipeline; and

storing ~~an~~ the override signal in a bit location of a bypass register.

10. (CURRENTLY AMENDED) The method as in claim 6, further comprising:

storing computer code in a memory, said computer code having a code entry point selected by said data bypass circuit to enable a downstream processor to do the work of ~~a~~ the failed processor.

11. (CURRENTLY AMENDED) Apparatus for enhancing debug capability in a multiprocessor circuit, comprising:

means for advancing data among a plurality of processors, ~~the plurality of processors arranged so that data advances from processor to processor~~ during normal operation in response to completion signals from each of the processors;

means for advancing data among the processors ~~by an advancement circuit,~~ in the event of failure of a processor in response to an override signal; and

means for passing the data through a processor complex including the ~~past a~~ failed one of the processors by moving data from a first context memory to a second context memory of the processor complex absent processing ~~a data bypass circuit~~.

12. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

means for indicating that a processor is to be bypassed ~~by a bypass register~~.

13. (PREVIOUSLY PRESENTED) The apparatus as in claim 11, further comprising:

means for arranging said plurality of processors to process data as a pipeline.

14. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

means for arranging said plurality of processors to process data as a pipeline; and

means for storing an override signal in a bit location of a bypass register.

15. (CURRENTLY AMENDED) The apparatus as in claim 11, further comprising:

means for storing computer code ~~in a memory~~, said computer code having a code entry point selected ~~by said data bypass circuit~~ to enable a downstream processor to do the work of a failed processor.

16-17. (CANCELLED)

18. (NEW) Logic encoded on one or more tangible media for execution, and when executed operable to:

advance data among a plurality of processors during normal operation in response to completion signals from each of the processors;

advance data among the processors in the event of failure of a processor in response to an override signal; and

pass data through a processor complex including the failed one of the processors by moving data from a first context memory to a second context memory of the processor complex absent processing.